

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WALTER C. BONNEAU Jr., KARL M. GUTTAG and ROBERT J.
GOVE

Appeal No. 1996-3669
Application No. 08/274,132¹

ON BRIEF

Before MARTIN, BARRETT and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 13-16, 18-24, and 26-29, all of the claims pending in

¹ Application for patent filed July 12, 1994. According to appellants, the application is a continuation of Application No. 07/813,857, filed December 26, 1991, now abandoned.

Appeal No. 1996-3669
Application No. 08/274,132

the application. Claims 1-12, 17, 25, and 30-34 have been canceled.

The claimed invention relates to a method of manufacturing integrated circuits using an architecture having multiple processors and multiple memories. More particularly, Appellants indicate at page 4 of the specification that the modular characteristic of the architecture enables the integrated circuit to have a majority of the same address and data pin-outs regardless of the number of processors on the chip.

Claim 13 is illustrative of the invention and reads as follows:

13. A method of manufacturing integrated circuits using semiconductor chips, comprising the steps of:

- a. making an architecture having multiple instances of a modular unit including a processor, a memory and a crossbar link disposed therebetween, said crossbar links of said modular units connected together providing direct communication between any processor and any memory of a predetermined number of said multiple modular units, and having input/output pads for connecting said architecture to external circuits;

Appeal No. 1996-3669
Application No. 08/274,132

- b. grouping said modular units into at least first and second groups, including in each group at least one said modular units;
of
- c. selecting a first desired number of modular units
for a first integrated circuit;
- d. slicing said architecture between any two groups, to give said selected number of modular units;
- e. repositioning said input/output pads;
- f. terminating said connection between crossbar links
at said slicing between said two groups;
- g. constructing an integrated circuit having said
selected first desired number of modular units; and
- h. repeating steps d, e, f and g for a second desired number of processors,
wherein said first desired number of processors is different from said second desired number of processors, and wherein said integrated circuits have a majority of the same address and data pin-outs, regardless of said number of modular units chosen.

The Examiner relies on the following prior art:

Seefeldt et al. (Seefeldt)	4,978,633	Dec. 18, 1990
Balmer et al. (Balmer)	5,226,125	Jul. 06, 1993
(filed Nov. 17, 1989)		

Appeal No. 1996-3669
Application No. 08/274,132

Claims 13-16, 18-24, and 26-29 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over the combined teachings of Seefeldt and Balmer.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer. It is our view, after consideration of the record before us, that the collective evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the

Appeal No. 1996-3669
Application No. 08/274,132

art the obviousness of the invention as set forth in claims 13-16, 18-24, and 26-29. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577,

Appeal No. 1996-3669
Application No. 08/274,132

221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to independent claims 13 and 24, the Examiner proposes to combine the modular architecture teachings of Seefeldt with the single chip processor, memory, and crossbar link architecture of Balmer. In the Examiner's view (Answer, page 9), the skilled artisan would be motivated to make the combination to enable the efficient production of the Balmer architecture on a semiconductor wafer.

Upon careful review of the applied prior art in light of the arguments of record, we are in agreement with Appellants' stated position that the proposed combination of Seefeldt and Balmer does not make obvious the claimed subject matter. In our view, the Examiner has combined the general teachings of a modularly constructed gate array in Seefeldt and a single chip processor-memory configuration in Balmer in some vague manner without specifically describing how the teachings would be combined. This does not persuade us that one of ordinary skill in the art having the references before her or him, and

using her or his own knowledge of the art, would have been put in possession of the claimed subject matter. For example, in attempting to address the claim language relating to address and data pin-outs, the Examiner points to the Figure 57 illustration and accompanying description at column 12 of Balmer. From this description, the Examiner asserts the "belief" that the address and data pin-outs are the same regardless of the number of processors or memories. We note that the Examiner has provided no basis on the record that would support such a conclusion. In any case, regardless of the merits of such an interpretation of the teachings of Balmer, no convincing reasoning has been supplied by the Examiner as to how or why the skilled artisan would apply such teachings to Seefeldt. As correctly pointed out by Appellants, Balmer's system is a fixed design with no suggestion of modular expansion appearing in the disclosure.

In addition, the Examiner does not explain why the skilled artisan would have been motivated to modify Seefeldt to provide processor/memory architecture since Seefeldt is directed to a gate array structure which does not require

Appeal No. 1996-3669
Application No. 08/274,132

memory addressability capability. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n. 14 (Fed. Cir. 1992). None of the problems sought to be overcome by Balmer would be expected to exist in Seefeldt. We are left to speculate why the skilled artisan would modify the existing circuitry of Seefeldt to provide for the processors, memories, and cross-bar connections suggested by Balmer. The only reason we can discern is improper hindsight reconstruction of Appellants' claimed invention. Accordingly, since the Examiner has not established a prima facie case of obviousness, the 35 U.S.C. § 103 rejection of independent claims 13 and 24, and claims 14-16, 18-23, and 26-29 dependent thereon, cannot be

Appeal No. 1996-3669
Application No. 08/274,132

sustained. Therefore, the decision of the Examiner rejecting
claims 13-16, 18-24, and 26-29 is reversed.

REVERSED

JOHN C. MARTIN)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
JOSEPH F. RUGGIERO)	
Administrative Patent Judge)	

jrg

Appeal No. 1996-3669
Application No. 08/274,132

Robert D. Marshall Jr.
Texas Instruments Incorporated
Patent Department
P.O. Box 655474 MS 219
Dallas, TX 75262

Appeal No. 1996-3669
Application No. 08/274,132